REMARKS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-5 and 7-12 are pending in this application. No claims have been amended, canceled, or added by the present amendment.

In the outstanding Office Action, the title was objected to; Claims 1-5 stand rejected under 35 U.S.C. §102(b) as allegedly being anticipated by Huang (U.S. Patent No. 5,963,609, hereafter "Huang"); Claims 1-5, 7-8 and 12 stand rejected under 35 U.S.C. §102(b) as allegedly being anticipated by Goetz (U.S. Patent No. 5,233,615, hereafter "Goetz"); and Claims 9-11 stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Huang and further in view of Banman (U.S. Patent No. 5,557,751, hereafter "Banman").

Regarding the objection to the title, the title has been amended to be more descriptive as suggested by the outstanding Office Action. No new matter has been added. Accordingly, it is respectfully requested this objection be withdrawn.

The outstanding rejections on the merits of the claims are traversed for at least the following reasons.

Briefly recapitulating, independent Claim 1 is directed to a processor array that includes an array of processor elements. Claim 1 recites, among other things, that:

> each processor element being such that, on receipt of a control command signal, it acts on that signal only when its cycle counter reaches a predetermined value, and

said one of said processor elements being such that it transmits control command signals only when its cycle counter takes a value which is within a predetermined range.

In the following, the above claimed two features are referred to as feature (1) and feature (2). Independent Claims 11 and 12 also include features (1) and (2).

The processor array of Claim 1 advantageously synchronizes the execution of commands in a parallel processor array. In such an array, one processor (a master) may issue commands to all of the other processors (slaves), which are intended to be operated at the same time. Because some slaves have shorter data paths from the master than other slaves, these slaves may receive the command at different times, and thus execute the command at different times.

The device of Claim 1 is configured such that each slave waits until a predetermined number of clock cycles has passed before acting on the received command signal. In this way, slaves near the master, which receive the command quicker than other slaves, wait a longer time than slaves farther away from the master. However, due to claimed feature (1) all the slaves execute the command at the same time.

Further, there is a "safe window" during each processing cycle during which commands can be issued by the master. The "safe window" recited by feature (2) prevents the following two situations. If the master issues a command too soon in the cycle, the command will be received by the nearby slaves before they have executed a previous command. However, if the master waits too long to send the command out, the command will not be received by the far away slaves in time.

Thus, the master is configured to only transmit new command signals during a certain portion of the processing cycle, as recited by feature (2).

Turning to the applied art, Huang teaches an apparatus for serial data communication between a plurality of chips. One chip acts as a master and, in response to a transfer request, the master generates a "transfer control signal" and a "synchronization clock signal," which are transmitted to the slaves as disclosed at column 5, lines 40-49.

More specifically, Huang discloses that when the master transmits the transfer control signal, all the processors start counting the clock cycles and only then, the processors transfer data according to a predefined protocol. That is, after receiving the transfer control signal, processor A transmits data to processor B during a first period, then processor A transmits data to processor C during a second period, and so on until each processor has transmitted data to each other processor.

In this regard, Figure 4 shows the transfer control signal and the synchronizing clock signal sent by the master to the processors. The transfer control signal has two phases, an idle phase and a transfer phase. During the idle phase, no synchronizing clock signal is sent to the slaves. Only in the transfer phase the synchronizing clock signal is transferred to the slaves, as described by Huang at column 5, lines 40-50. Further, Huang discloses at column 5, line 51 to column 6, line 4, that "... during a transfer phase which starts at the time T_1 and ends at the time T_7, there are five intervals during which data can be transferred, i.e., the intervals T_1-T_2, T_2-T_3, T_3-T_4, T_4-T_5, and T_5-T_6." The five intervals are allocated for the

transfer of five bits, Bit 0 to Bit 4, each of them indicating "data transmission" from one chip to another chip.

Huang does not teach or suggest claimed feature (1)

Huang discloses two distinct transfers, a first one being the **transfer control signal** from the master to the slaves and a second one being the **data transmission** among the processors. While the **data transmission** is controlled by a counter the **transfer control signal** is not in the device of Huang.

Therefore, Applicants respectfully submit that the outstanding Office Action mistakenly corresponds the claimed "control command signal" with the "data transmission" of Huang, and for this reason, Huang does not teach or suggest feature (1).

Huang does not teach or suggest claimed feature (2)

Regarding claimed feature (2), the outstanding Office Action refers to column 3, lines 25—34 of Huang for disclosing this feature and states that each transmitter and receiver can only operate during specified cycle phases of a transfer phase. This paragraph of Huang discloses that once a transfer command has been issued, each processor (including the master) can only transfer data during a designated period. However, claimed feature (2) requires that the master processor, which transmits the control command signals, to only transmit control command signals

during a certain time range. A control command signal is, as recited by the independent claims, one that each processor will act upon when receiving.

The transfer control signal of Huang, which is transmitted by the master processor, is not disclosed to be transmitted "only when" the cycle counter of the master "reaches a predetermined value," as recited by the independent claims. The data transmission in Huang appears to be controlled by a cycle counter.

However, the data transmission of Huang cannot be associated with the claimed control command signal. Thus, as the passage referred to by the outstanding Office Action is not referring to the master issuing a transfer control signal but rather to transfer of what may be termed message data between the processors, that passage and any other passage of Huang do not anticipate or render obvious the claimed subject matter.

It is noted that in the "Response to Arguments" section at page 8, numbered paragraph 25 of the Final Action, it is acknowledged that Huang does not disclose a master device being restricted at certain period of times when it can send the transfer control signal but suggests that such limitation is not present in the claims.

Applicants disagree with this interpretation of the independent claims and respectfully submit that feature (2) of the independent claims recite that "said one of said processor elements [which is thus referring to the processor which transits control command signals] ... ***transmits control command signals only when*** its cycle counter ... is within a predetermined range" (emphasis added).

To further clarify that the master of Huang is different from claimed feature (2), it is noted that Huang discloses that the transfer control signal may be transmitted in response to a request from a slave chip or to internal conditions (see Huang, column 2, lines 48—50) and gives no indication at all that the master is restricted as to when it can transmit the transfer control signal.

Thus, there is no indication in Huang that the transfer control signal can only be transmitted during certain ranges of values of the cycle counter. The internal conditions referred to in Huang are simply the need to transfer data. Further, it will be noted that Huang suggests that the synchronisation clock is generated in response to a transfer request (column 2, lines 50—51). In this regard, Figure 4 shows that outside the transfer phase there is no transfer control signal and no synchronisation clock signal. If there is no synchronisation clock signal outside the transfer phase it is difficult to see how the master could transmit a control signal in response to a cycle counter counting the cycles of synchronisation signal.

In addition, Huang is not concerned with simultaneous processing of different processors and instead is concerned with time division of common data transfer buses. Thus, there is no teaching or suggestion in Huang regarding limiting the time at which transfer commands can be transmitted.

Therefore, it is respectfully submitted that the assumption of the outstanding Office Action in the paragraph bridging pages 2 and 3 that Huang discloses claimed features (1) and (2) is not accurate.

Accordingly, it is respectfully submitted that independent Claims 1, 11, and 12 and each of the claims depending therefrom patentably distinguish over Huang.

Regarding the rejection of the claims over Goetz, it is noted that Goetz does not teach a processor array in which one processor is able to transmit command control signals to each of the other processors. Goetz teaches that instead of using a single processor to perform a task, a multiplicity N of processors may be used to achieve fault tolerant operation. The N identical processors are programmed to each execute identical programs in response to a common set of input signals. As shown in Figure 1, each processor A, B and C is arranged to receive system inputs and pass their outputs to a majority voter, see for example description in Goetz at column 3, lines 7-22.

Therefore, each processor in Goetz is arranged to be independent of the other processors and to run an identical program for fault tolerance, which is contrary to the independent claims.

Further, Goetz does not teach or suggest a processor array where one processor is arranged to transmit control commands to the other processors. On the contrary, Goetz teaches away from such an arrangement as no master or slaves are established in the system.

The outstanding Office Action refers to interrupt signals in Goetz as corresponding to the claimed command control signals. However, Figure 2 of Goetz shows that the cyclic interrupt signal is generated externally of any of the processors,

and column 3, lines 56 — 61 discloses that the cyclic interrupt is generated from a master timing source which is different from the processors.

It is further noted that the cyclic interrupt signal of Goetz, not being transmitted by a processor of the array, cannot include the "synchronization control command" transmitted by one of the processor recited in Claim 1.

Accordingly it is respectfully submitted that independent Claims 1, 11, and 12 and each of the claims depending therefrom patentably distinguish over Goetz.

Regarding the rejection of independent Claim 11 under 35 USC § 103(a) as unpatentable over Huang in view of Banman, this rejection is respectfully traversed for at least the following reasons.

As discussed above, independent Claim 11 recites features similar to Claim 1, which are not disclosed by Huang. The outstanding Office Action states on page 8, first full paragraph, that Huang "does not explicitly disclose storing transferred data in registers corresponding to the predetermined sequence of code words such that each received word is stored in its respective register for the duration of said predetermined sequence of code words." In order to cure only this deficiency of Huang, the outstanding Office Action relies on Banman.

However, Banman does not cure the other deficiencies discussed above with regard to Huang. Accordingly it is respectfully submitted that independent Claim 11 patentably distinguishes over Huang and Banman, either alone or in combination.

Subsequently, in light of the above discussion, the present application is believed to be in condition for allowance and an early and favorable action to that effect is respectfully requested. Should the Examiner have any questions relating to expediting the prosecution of this application, he is urged to contact the undersigned at the number provided below.

Respectfully submitted,

POTOMAC PATENT GROUP PLLC

By: /Remus F. Fetea/
Remus F. Fetea, Ph.D.
Registration No. 59,140

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Potomac Patent Group, PLLC
P.O. Box 270
Fredericksburg, VA 22404
(540) 361-2601